

DATA SHEET

RFX8053: CMOS 5 GHz WLAN 802.11ac RFelC with PA, LNA, and SPDT

Applications

- 802.11a/n/ac WiFi devices
- Smartphones
- Tablets/MIDs
- Gaming
- Consumer electronics
- Notebooks/netbooks/ultrabooks
- Mobile/portable devices
- Other 5 GHz ISM platforms

Features

- 5 GHz WLAN single-chip, single-die RF front-end IC
- High transmit signal linearity meeting standards for 802.11ac ODFM/MCS9 modulation
- Separate TX and RX transceiver port and single antenna port
- 5 GHz power amplifier with low-pass harmonic filter
- Low-noise amplifier with bypass mode
- Transmit/receive switch circuitry
- Integrated power detector for transmit power monitor and control
- Low voltage (1.2 V) CMOS control logic
- Very low DC power consumption
- ESD protection circuitry on all pins
- DC decoupled RF ports
- Internal RF decoupling on all VDD bias pins
- Low noise figure for the receive chain
- High power capability for received signals in bypass mode
- Full on-chip matching circuitry
- Minimal external components required
- 50 Ω input/output matching
- Market-proven CMOS technology
- Small QFN (16-lead, 2.5 x 2.5 x 0.45 mm) package with exposed ground pad

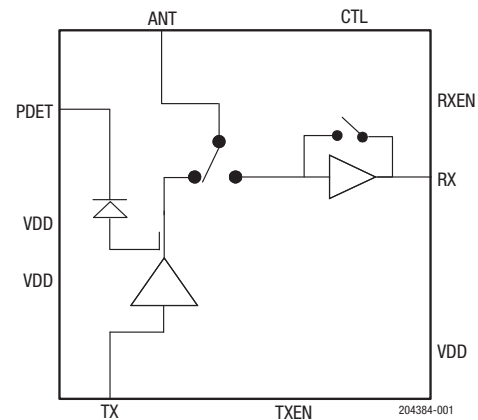


Figure 1. RFX8053 Block Diagram

Description

The RFX8053 is a highly integrated, single-chip, single-die RFelC (RF Front-end Integrated Circuit) that incorporates key RF functionality for IEEE 802.11a/n/ac WLAN systems operating in the 5.15 to 5.825 GHz range. The RFX8053 architecture integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters in a CMOS single-chip device.

The RFX8053 has simple and low-voltage CMOS control logic that requires minimal external components. A directional coupler-based power detect circuit is integrated for accurate monitoring of output power from the PA.

The RFX8053 is an ultra-compact low-profile 2.5 x 2.5 x 0.45 mm 16-lead QFN package. With support to direct battery operation, the RFX8053 is an ideal RF front-end solution for implementing 5 GHz WLAN in smartphones and other platforms.



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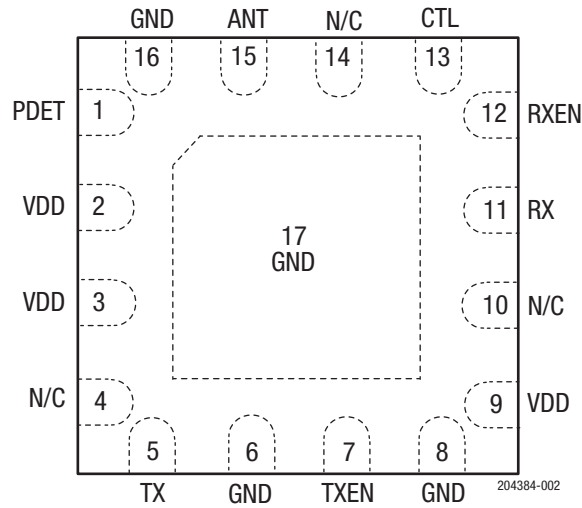


Figure 2. RFX8053 Pinout (Top View)

Table 1. RFX8053 Signal Descriptions

| Pin | Name | Description | Pin | Name | Description |
|--------------|------|--|-----|------|--|
| 1 | PDET | Analog voltage proportional to the PA power output | 7 | TXEN | CMOS input to control TX enable |
| 2, 3, 9 | VDD | DC supply voltage | 11 | RX | RF output port from LNA or bypass – DC shorted to GND |
| 4, 10, 14 | N/C | Not connected internally | 12 | RXEN | CMOS input to control RX enable |
| 5 | TX | RF input port from the transceiver – DC shorted to GND | 13 | CTL | CMOS input for additional TX control |
| 6, 8, 16, 17 | GND | Ground – must be connected to GND in the application circuit | 15 | ANT | Antenna port RF signal from the PA or RF signal applied to the LNA or bypass – DC shorted to GND |

Electrical and Mechanical Specifications

The absolute maximum ratings of the RFX8053 are provided in Table 2. The recommended operating conditions are specified in Table 3.

The electrical specifications are provided in Tables 4 and 5. The state of the RFX8053 is determined by the logic provided in Table 6.

Table 2. RFX8053 Absolute Maximum Ratings¹

| Parameter | Conditions | Minimum | Maximum | Units |
|--|--|---------|---------|-------|
| DC VDD voltage supply | All VDD pins | 0 | 5.5 | V |
| DC control pin voltage | All control pins | 0 | 3.6 | V |
| DC VDD current consumption | Through VDD pins when TX is ON | | 400 | mA |
| TX RF input power | | | +7 | dBm |
| ANT RF input power | Bypass mode | | +10 | dBm |
| Junction temperature | | | 150 | °C |
| Storage ambient temperature | Appropriate care required according to JEDEC Standards | -40 | +150 | °C |
| Operating temperature | Case temperature | -40 | +85 | °C |
| Electrostatic discharge: Human Body Model (HBM) | | 1000 | | V |

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device. All maximum RF input power ratings assume 50 Ω terminal impedance.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. RFX8053 Recommended Operating Conditions

| Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------------|-----------------------------------|-----|-----|-----|-------|
| DC VDD voltage supply ¹ | All VDD pins | 3.0 | 3.6 | 4.8 | V |
| Control voltage high ² | 3.6 V or VDD (whichever is lower) | 1.2 | | | V |
| Control voltage low | | 0 | | 0.3 | V |
| DC control pin current consumption | | | 1 | | µA |
| DC shutdown current | | | 3 | 10 | µA |
| PA turn-on/turn-off time | | | | 0.4 | µsec |
| θ _{ja} ³ | | | 28 | | °C/W |
| θ _{ja} | | | 44 | | °C/W |
| LNA switch speed | | | | 0.4 | µsec |

¹ For normal operation of the RFX8053, VDD must be continuously applied to all VDD supply pins.

² If control voltage can exceed 1.8 V, a 1 kΩ to 10 kΩ series resistor is recommended for the application circuit on each control line.

³ Thermal measurements were performed on a test EVB under typical use conditions. Please contact Skyworks for details regarding the test conditions and the configuration of the thermal vias on the EVB. Refer to the PCB Land Pattern in Figure 3 for recommended thermal vias.

Table 4. RFX8053 Transmit Electrical Characteristics (VDD = 3.3 V, TA = +25°C, Unless Otherwise Specified)

| Parameter | Test Condition | Min | Typ | Max | Units |
|--|--|-------|-------|-------|-------|
| Operating frequency band | | 5.15 | | 5.825 | GHz |
| Linear output power for 802.11ac | DEVM –35 dB, 802.11ac, MCS9, VHT80 | +14.5 | +15.5 | | dBm |
| Linear output power for 802.11n | EVM –32 dB, 802.11n, MCS7, HT40 | | +18 | | dBm |
| Linear output power for 802.11a | EVM 3.5%, 802.11a, QAM 64, 54 Mbps | | +19 | | dBm |
| Linear output power for 802.11a, 6 Mbps | For 802.11a 6 Mbps mask compliance | | +21 | | dBm |
| Small-signal power gain | Between TX and ANT pins | | 28 | | dB |
| Gain flatness | Between 5.15 and 5.85 GHz | | ±1 | | dB |
| TX quiescent current | | | 210 | | mA |
| TX linear current | POUT = +18 dBm | | 270 | | mA |
| Out-of-band rejection | At 3.9 to 7.2 GHz, relative to in-band gain | -10 | -15 | | |
| Power detector voltage output | POUT = +5 to +20 dBm, 10 kΩ load | 300 | | 1600 | V |
| Second harmonic | POUT=+19 dBm, C/W | | -35 | | dBc |
| Third harmonic | POUT=+19 dBm, C/W | | -50 | | dBc |
| Input return loss | At TX port | | -10 | | dB |
| Output return loss | At ANT port | | -10 | | dB |
| Load VSWR for stability (CW, fix pin for POUT = +21 dBm with 50 Ω load) | All non-harmonically related spurs less than -43 dBm/MHz | 4:1 | 6:1 | | N/A |
| Load VSWR for ruggedness (CW, fix pin for POUT = +21 dBm with 50 Ω load) | No damage | 8:1 | 10:1 | | N/A |

Table 5. RFX8053 Receive Electrical Characteristics (VDD = 3.3 V, TA = +25°C, Unless Otherwise Specified)

| Parameter | Test Condition | Min | Typ | Max | Units |
|------------------------------------|---|------|-------|------|-------|
| Operating frequency band | All RF pins loaded by 50 Ω | 5.15 | | 5.85 | GHz |
| Gain | High-gain mode, between ANT and RX pins, RXEN = high, CTL = low | 10 | 12 | | dB |
| Noise figure | High-gain mode, at ANT pin | | 3.1 | | dB |
| Insertion loss for LNA bypass mode | Between ANT and RX pins; RXEN = low, CTL = low | | 5 | | dB |
| Input return loss | At ANT port, high-gain mode | | -6 | | dB |
| | Bypass mode | | -10 | | |
| Output return loss | At RX port, high-gain mode | | -6 | | dB |
| | Bypass mode | | -8 | | |
| RF port impedance | | | 50 | | Ω |
| DC quiescent current | No RF applied, through VDD, high-gain mode | | 16 | | mA |
| | No RF applied, through VDD, bypass mode | | 0.003 | | |
| IIP3 | At ANT pin, high-gain mode | | +6 | | dBm |
| | At ANT pin, bypass mode | | +20 | | |

Table 6. RFX8053 Control Logic¹

| Mode of Operation | TXEN | LEN | RXEN |
|-------------------------|------------|-----|------|
| Receive Bypass Mode | 0 | 0 | 0 |
| Receive Mode, High-Gain | 0 | 0 | 1 |
| Transmit Mode | 1 | X | 0 |
| Not specified | All others | | |

¹ "1" denotes high voltage state (> 1.2 V)
 "0" denotes low voltage stage (< 0.3 V) at control pins
 "X" denotes do not care: high or low state
 1 kΩ – 10 kΩ series resistor may be required for each control line.

Package Dimensions

The PCB layout footprint for the RFX8053 is shown in Figure 3. The typical part marking is shown in Figure 4. Package dimensions are shown in Figure 5. Tape and reel dimensions are provided in Figure 6.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The RFX8053 is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

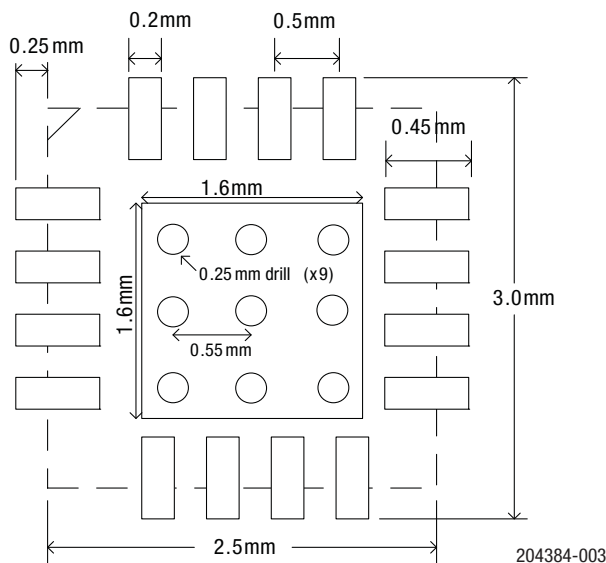


Figure 3. RFX8053 PCB Layout Footprint

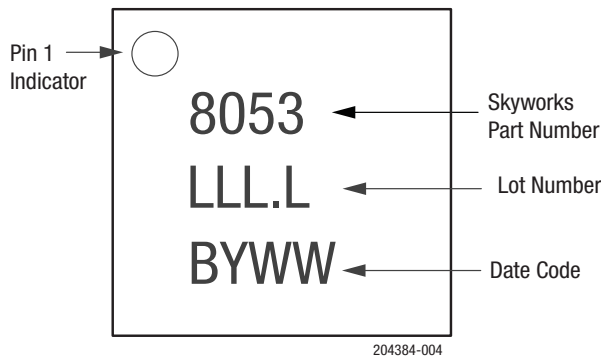
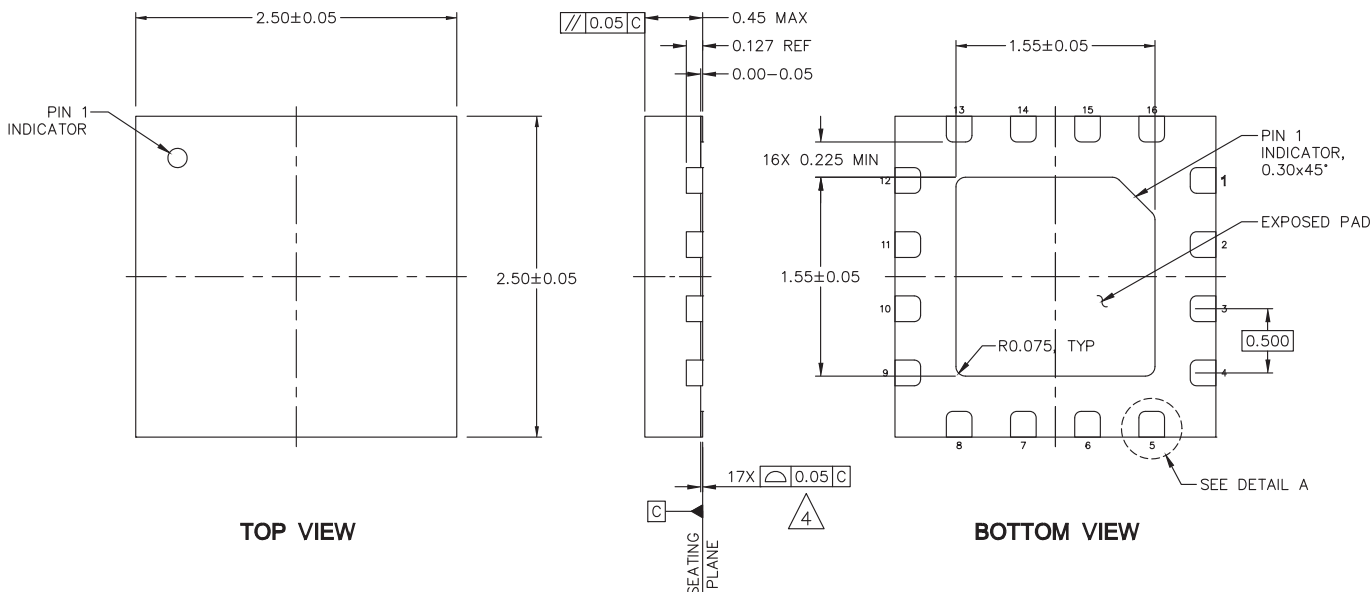
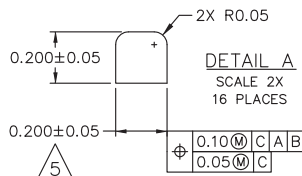


Figure 4. Typical Part Markings (Top View)



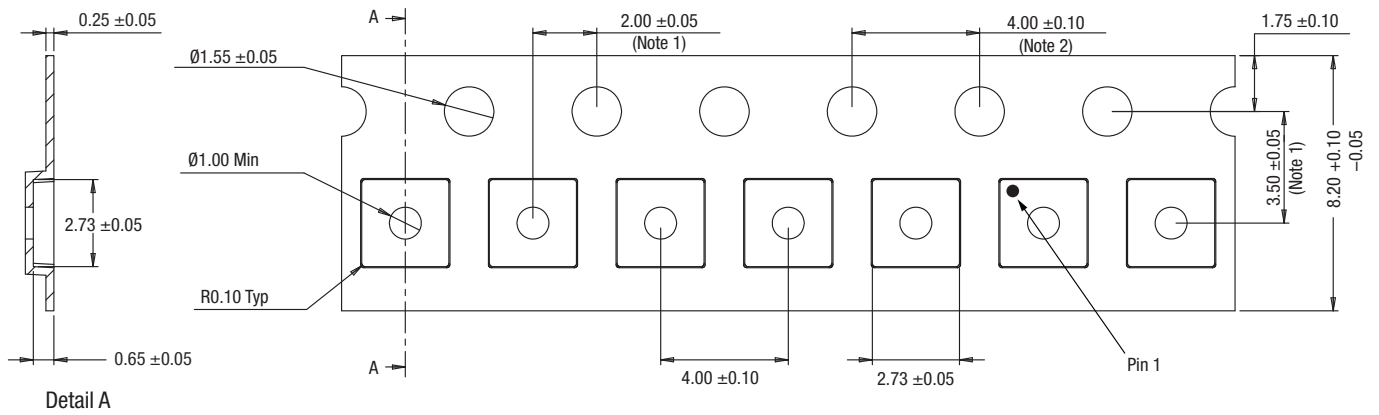
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 2. DIMENSIONS ARE IN MILLIMETERS.
 3. TOLERANCING (UNLESS OTHERWISE SPECIFIED):

| | |
|-------------------------|--------------------|
| DECIMAL TOLERANCE: | ANGULAR TOLERANCE: |
| X.X (1 PLC) ± 0.1mm | ± 1/2° |
| X.XX (2 PLC) ± 0.05mm | |
| X.XXX (3 PLC) ± 0.025mm | |
 4. COPLANARITY APPLIES TO THE TERMINALS AS WELL AS ALL OTHER BOTTOM SURFACE METALLIZATION.
 5. DIMENSION APPLIES TO METALIZED TERMINAL. IF TERMINAL TIP HAS A RADIUS, DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
 6. PLATING REQUIREMENTS PER SOURCE CONTROL DRAWING (SCD) 2504.
 7. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES.



204384-005

Figure 5. RFX8053 Package Dimensions



Notes:

1. Measured from center line of sprocket hole to center line of pocket.
2. Cumulative tolerance of 10 sprocket holes = ± 0.10 mm.
3. Other material available.
4. All dimensions are in millimeters.

204384-006

Figure 6. RFX8053 Tape and Reel Dimensions

Ordering Information

| Model Name | Manufacturing Part Number | Evaluation Board Part Number |
|--|---------------------------|------------------------------|
| RFX8053: CMOS 5 GHz WLAN 802.11ac RFEIC with PA, LNA, and SPDT | RFX8053 | RFX8053-EK1 |

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